



SiPS 2016

IEEE Workshop on Signal Processing Systems
Dallas, Texas, Oct. 26-28 2016

<http://sips2016.rice.edu>



General Chairs

Marilyn Wolf
Georgia Institute of Technology, USA
Manish Goel
Samsung Mobile Processor Innovation Lab, USA

SiPS is a major international forum for discussion of new technology progress and innovations in the design and implementation of digital signal processing systems. It addresses all aspects of architecture and design methods of these systems. Emphasis is on current and future challenges in research and development in both academia and industry. Prospective authors are invited to submit manuscripts on topics including, but not limited to:

Paper submission deadline: May 2

Program Chairs

Joe Cavallaro
Rice University, USA
Zhongfeng Wang
Broadcom, USA

Acceptance notification: July 18

VLSI Based Design and Implementation of Signal Processing Systems

- Low-power signal processing circuits and applications
- High performance VLSI systems
- VLSI design for 100 Gbps and beyond networking systems
- FPGA and reconfigurable architecture based systems
- System-on-chip and network-on-chip
- VLSI Systems for Wireless Sensor Network and RF Identification Systems

Camera ready paper due: August 8

Signal Processing Application Systems

- Audio, speech and language processing
- Biomedical signal processing and bioinformatics
- Image, video and multimedia signal processing
- Information forensics, security and cryptography
- Machine learning for signal processing
- Sensing and sensor signal processing
- Autonomous energy harvesting-based sensor networks
- Signal processing for non-volatile memory systems
- Latency and power constrained signal processing techniques for high-speed networking
- Wireless communications and networking
- Coding and Compression
- Multiple-Input-Multiple-Output (MIMO) and Communication Systems
- Software Defined Radio

Finance Chair

Seok-Jun Lee
Samsung Mobile Processor Innovation Lab, USA

Software Based Design and Implementation of Signal Processing Systems

- Programmable digital signal processor architecture and systems
- Application specific instruction-set processor (ASIP) architecture and systems
- SIMD, VLIW and multi-core CPU architecture
- Graphic processing unit (GPU) based massively parallel implementation
- Embedded FPGA architectures

Emerging Technologies

- Vehicular ad hoc networks (VANET)
- Cognitive radio networks
- Internet of Things (IoT)
- Deep learning and reconfigurable/ASIC processors
- Bio-inspired networks
- Context-aware mobile networking
- Wireless body area networks (WBANs)
- Implantable Communications
- Tele-medicine/e-health networks

Local Program Chair

Sridhar Rajagopal
Samsung R&D Lab, USA

Signal Processing Compensation Techniques for Analog and Digital VLSI

- Digital Compensation techniques for variations in Silicon process, temperature, aging
- Error Detection and Correction for Volatile and Non Volatile Memories
- Power Reduction and SNR Improvement for On-chip, off-chip interconnects and buses
- Digital Compensation Signal Processing for ADCs, power-amps, MEMS, power Controllers

Design Methods of Signal Processing Algorithms and Architectures

- Optimization of signal processing algorithms
- Compilers and tools for signal processing systems
- Algorithm transformation and algorithm-to-architecture mapping
- Error-Tolerant Techniques for Signal Processing

Local Arrangements Chairs

Rama
Venkatashubramanian Texas Instruments, USA
Issa Panahi
UT Dallas, USA
Wanda Gass
High Tech High Heels, USA

Sponsored by:

- IEEE Signal Processing Society
- IEEE Circuits and Systems Society
- Samsung

Paper Submission: Authors are invited to submit full-length (6 pages maximum), original, unpublished papers. Previously published papers or papers currently under review for other conferences/journals should not be submitted and will not be considered. Paper format information is available at <http://sips2016.rice.edu>.

In 2016, SiPS's special theme is on "Signal processing beyond performance optimization." Future Signal Processing applications will have to consider processing latency and power constraints in addition to pursuing optimal system performance. The fundamental dilemma is that the complexity of SP is rapidly increasing to improve system performance while target data-rate of real applications increase exponentially. Submissions that fall into this inter-disciplinary area are particularly encouraged.

Student Paper Contest and Special Issue: There will be a contest for best student papers, and selected papers will be considered for publication in a special issue of the Journal of Signal Processing Systems.